ABSTRACT OF THE INVENTION

A stackable layer and stacked multilayer module are disclosed. Individual integrated circuit die are tested and processed at the wafer level to create vertical area interconnect vias for the routing of electrical signals from the active surface of the die to the inactive surface. Vias are formed at predefined locations on each die on the wafer. The wafer is passivated and the vias are filled with a conductive material. The bond pads on the die are exposed and a metalization reroute from the user-selected bond pads and vias is applied. The inactive surface of the wafer may be back thinned if desired. The wafer is then segmented to form thin, stackable layers that can be stacked and vertically electrically interconnected using the conductive vias, forming high-density electronic modules which may, in turn, be further stacked and interconnected to form larger more complex stacks.